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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,043	08/18/2003	Scott D. Brandenburg	DP-308286	3075

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EXAMINER	
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ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,043	BRANDENBURG ET AL	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/23/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *21-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/643043 Attorney's Docket #: DP-308286
Filing Date: 8/13/2003;

Applicant: Brandenburg et al.

Examiner: Alexander Williams

Applicant's election of Group I (claims 1 to 20), filed 9/23/04, has been acknowledged.

This application contains claims 21 to 40 drawn to an invention non-elected without traverse. Applicant's request that claims 21-40 of Group II to be canceled without prejudice was not canceled in proper amendment to the claims form. If Applicant desired to cancel these claims at this time, a proper amendment is required.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities: In paragraph [0003], the co-pending U.S. Patent Application serial No. status information should be updated.

Appropriate correction is required.

The drawings are objected to because in figure 2, in the middle of the figure, "30" is misdirected to the element of the circuit device "12", rather than the solder joint, in which should be --30--.

Correction is required.

Claims 6 and 13 to 20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 6 and 13, it is unclear and confusing to what is meant by "wherein a thermally-conductive lubricant is not present between the second surface of the flip-chip device and the heat-conductive member." Weber defines 'lubricant" as a usually oily substance, as grease, that reduces friction, heat, and wear, when applied as a surface coating to moving parts or between solid surfaces. Weber defines "solder" as any of various fusible, usually tin and lead alloys used to join metallic parts when applied in the melted state to the solid metal. Something that joins or cements. To function as a bond between; join. To unite or repair objects with solder. Applicant claim "a solder joint." Can this be considered "a thermally-conductive lubricant" when solder is in the liquid or melted state?

Any of claims 6 and 13 to 20 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 6, 9, 11 and 12, **insofar as claim 6 can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Turlik et al. (U.S. Patent # 5,325,265).

1. Turlik et al. (figure 1) show an electronic assembly **10** comprising: a housing member **26** comprising a heat-conductive member; a substrate **12** supported by the housing member, the substrate having conductors **17** on a surface thereof; a circuit device **20** mounted to the substrate with solder connections **34** on a first surface of the device that are registered with the conductors on the substrate, the device having a second surface **42** oppositely disposed from the first surface; and a solder joint **28** consisting essentially of indium **(see column 8, lines 50-63)** and optionally one or more alloying **(see column 8, lines 59-63)** constituents that increase the melting temperature of the solder joint above that of indium, the solder joint bonding the second surface of the device to the heat-conductive member.

2. The electronic assembly according to claim 1, Turlik et al. show wherein the solder joint **28** consists essentially of indium **(see column 8, lines 50-63)**.
6. The electronic assembly according to claim 1, Turlik et al. show wherein a thermally-conductive lubricant is not present between the second surface of the device and the heat-conductive member.
9. The electronic assembly according to claim 8, Turlik et al. show wherein an overmold compound does not encapsulate the substrate and the device.
11. The electronic assembly according to claim 1, Turlik et al. show wherein a portion of the housing member **26** defines the heat-conductive member.
12. The electronic assembly according to claim 1, Turlik et al. show wherein the assembly lacks any biasing means that contacts a surface of the substrate opposite the device and urges the device into contact with the heat-conductive member.

Claims 1, 2, 6 and 10 to 12, **insofar as claim 6 can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Ma et al. (U.S. Patent # 6,423,570 B1).
1. Ma et al. (figures 1 to 17) specifically figure 1 show an electronic assembly comprising: a housing member **142** comprising a heat-conductive member; a substrate **140** supported by the housing member, the substrate having conductors **124** on a surface thereof; a circuit device **102** mounted to the substrate with solder connections **108** on a first surface **106** of the device that are registered with the conductors on the substrate, the device having a second surface **114** oppositely disposed from the first surface; and a solder joint **115** consisting essentially of indium **(see column 4, lines 10-30)** and optionally one or more alloying **(see column 4, lines 15-21)** constituents that increase the melting temperature of the solder joint above that of indium, the solder joint bonding the second surface of the device to the heat-conductive member.
2. The electronic assembly according to claim 1, Ma et al. show wherein the solder joint consists essentially of indium **(see column 4, lines 10-30)**.

6. The electronic assembly according to claim 1, Ma et al. show wherein a thermally-conductive lubricant is not present between the second surface of the device and the heat-conductive member.
10. The electronic assembly according to claim 1, Ma et al. show wherein the heat-conductive member **142** is a pedestal **(extended portion of 142)** protruding from the housing member:
11. The electronic assembly according to claim 1, Ma et al. show wherein a portion of the housing member **142** defines the heat-conductive member.
12. The electronic assembly according to claim 1, Ma et al. show an assembly lacks any biasing means that contacts a surface of the substrate opposite the device and urges the device into contact with the heat-conductive member.

Claims 1, 2, 6-8, 11 and 12, **insofar as claim 6 can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Koopman et al. (U.S. Patent # 4,081,825).
1. Koopman et al. (figures 1A to 4) specifically figure 1 show an electronic assembly comprising: a housing member **8** comprising a heat-conductive member; a substrate **4** supported by the housing member, the substrate having conductors **(see column 3, lines 13-22)** on a surface thereof; a circuit device **2** mounted to the substrate with solder connections **6** on a first surface of the device that are registered with the conductors on the substrate, the device having a second surface oppositely disposed from the first surface; and a solder joint **10** consisting essentially of indium **(see column 3, line 39 to column 4, line28)** and optionally one or more alloying constituents that increase the melting temperature of the solder joint above that of indium, the solder joint bonding the second surface of the device to the heat-conductive member.
2. The electronic assembly according to claim 1, Koopman et al. show wherein the solder joint consists essentially of indium.
6. The electronic assembly according to claim 1, Koopman et al. show wherein a thermally-conductive lubricant is not present between the second surface of the device and the heat-conductive member.

7. The electronic assembly according to claim 1, Koopman et al. further comprising an overmold compound that encapsulates the substrate and the device on the housing member.
8. The electronic assembly according to claim 1, Koopman et al. further comprising a cover member that, with the housing member, encloses the substrate and the device.
11. The electronic assembly according to claim 1, Koopman et al. show wherein a portion of the housing member defines the heat-conductive member.
12. The electronic assembly according to claim 1, Koopman et al. show wherein the assembly lacks any biasing means that contacts a surface of the substrate opposite the device and urges the device into contact with the heat-conductive member.

Claims 1, 2, 6, 8-13 and 18-20, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Patel (U.S. Patent # 5,396,403).
1. Patel (figures 1 to 4) specifically figure 4 show an electronic assembly comprising: a housing member **75,83,71,79** comprising a heat-conductive member **71,79**; a substrate **61** supported by the housing member, the substrate having conductors **(inherit)** on a surface thereof; a circuit device **63** mounted to the substrate with solder connections **(shown, but not labeled between 61 and 63)** on a first surface of the device that are registered with the conductors on the substrate, the device having a second surface oppositely disposed from the first surface; and a solder joint **73** consisting essentially of indium **(see column 6, lines 8-10)** and optionally one or more alloying constituents that increase the melting temperature of the solder joint above that of indium, the solder joint bonding the second surface of the device to the heat-conductive member.
2. The electronic assembly according to claim 1, Patel show wherein the solder joint consists essentially of indium.
6. The electronic assembly according to claim 1, Patel show wherein a thermally-conductive lubricant is not present between the second surface of the device and the heat-conductive member.

8. The electronic assembly according to claim 1, Patel further comprising a cover member **75,83** that, with the housing member **14**, encloses the substrate and the device.

9. The electronic assembly according to claim 8, Patel show wherein an overmold compound does not encapsulate the substrate and the device.

10. The electronic assembly according to claim 1, Patel show wherein the heat-conductive member **71** is a pedestal protruding **(71 connected to 75 through 77)** from the housing member.

11. The electronic assembly according to claim 1, Patel show wherein a portion of the housing member defines the heat-conductive member.

12. The electronic assembly according to claim 1, Patel show wherein the assembly lacks any biasing means that contacts a surface of the substrate opposite the device and urges the device into contact with the heat-conductive member.

13. Patel (figures 1 to 4) specifically figure 4 show an electronic assembly comprising: a housing **14,75,83** having an interior region; a heat-conductive pedestal **71** projecting into the interior region of the housing **(71,79 connected to 75,83 through 77,85)**; a laminate substrate **61** within the interior region of the housing and supported by the housing, the substrate having conductors **(inherit)** on a surface thereof; a flip-chip device **63** mounted to the substrate with solder connections **(shown but not labeled between 63 and 61)** on a first surface of the flip-chip device that are registered with the conductors on the substrate, the flip-chip device having a second surface oppositely disposed from the first surface; and a solder joint **73** consisting essentially of indium **(see column 6, lines 8-10)** and at least one alloy constituent that increases the melting temperature of the solder joint above that of indium, the solder joint bonding the second surface of the flip-chip device to the heat-conductive pedestal; wherein a thermally-conductive lubricant is not present between the second surface of the flip-chip device and the heat-conductive member.

18. The electronic assembly according to claim 13, Patel show wherein the housing **14** comprising a base member **83** and a cover member **75** that enclose the substrate **61** and the flip-chip device **63**.

19. The electronic assembly according to claim 18, Patel show wherein an overmold compound does not encapsulate the substrate and the flip-chip device.
20. The electronic assembly according to claim 13, Patel show wherein a portion of the housing **14,75,83** defines the pedestal **(71,79 connected to 75,83 through 77,85)**.

Claims 13 and 18 to 20, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Koors et al. (U.S. Patent # 6,180,436 B1) in view of Patel (U.S. Patent # 5,396,403).

13. Koors et al. (the figure) show an electronic assembly **10** comprising: a housing **14,20,22** having an interior region; a heat-conductive pedestal **26** projecting into the interior region of the housing; a laminate substrate **16** within the interior region of the housing and supported by the housing, the substrate having conductors **(see column 2, lines 64-67)** on a surface thereof; a flip-chip device **12** mounted to the substrate with solder connections **18** on a first surface of the flip-chip device that are registered with the conductors on the substrate, the flip-chip device having a second surface oppositely disposed from the first surface; and a solder joint **32**, the solder joint bonding the second surface of the flipchip device to the heat-conductive pedestal; wherein a thermally-conductive lubricant is not present between the second surface of the flip-chip device and the heat-conductive member, but fail to explicitly show a solder joint consisting essentially of indium and at least one alloy constituent that increases the melting temperature of the solder joint above that of indium. However, Weber defines 'lubricant" as a usually oily substance, as grease, that reduces friction, heat, and wear, when applied as a surface coating to moving parts or between solid surfaces. Weber defines "solder" as any of various fusible, usually tin and lead alloys used to join metallic parts when applied in the melted state to the solid metal. Something that joins or cements. To function as a bond between; join. To unite or repair objects with solder. Applicant claim "a solder joint" in which can be considered "a thermally-conductive lubricant" when solder is in the liquid or melted state.

Patel is cited for showing a hear sink assembly with thermally conductive plate for a plurality of integrated circuits on a substrate. Patel (figures 1 to 4) specifically figure 4 show an electronic assembly comprising: a housing **14,75,83** having an interior region; a heat-conductive pedestal **71** projecting into the interior region of the housing **(71,79 connected to 75,83 through 77,85)**; a laminate substrate **61** within the interior region of the housing and supported by the housing, the substrate having conductors **(inherit)** on a surface thereof; a flip-chip device **63** mounted to the substrate with solder connections **(shown but not labeled between 63 and 61)** on a first surface of the flip-chip device that are registered with the conductors on the substrate, the flip-chip device having a second surface oppositely disposed from the first surface; and a solder joint **73** consisting essentially of indium **(see column 6, lines 8-10)** and at least one alloy constituent that increases the melting temperature of the solder joint above that of indium, the solder joint bonding the second surface of the flip-chip device to the heat-conductive pedestal; wherein a thermally-conductive lubricant is not present between the second surface of the flip-chip device and the heat-conductive member for the purpose of improving ways of dissipating heat generated by the chips of a MCM with high levels of mechanical stress from differential expansion and ultimate failure of the solder connections to the chip.

18. The electronic assembly according to claim 13, either reference shows wherein the housing comprising a base member and a cover member that enclose the substrate and the flip-chip device.

19. The electronic assembly according to claim 18, either reference shows wherein an overmold compound does not encapsulate the substrate and the flip-chip device.

20. The electronic assembly according to claim 13, Koors et al. shows wherein a portion of the housing **14,26** defines the pedestal **26**.

Therefore, it would have been obvious to one of ordinary skill in the art to use Patel's solder joint to modify Koors et al.'s solder joint for the purpose of improving ways of dissipating heat generated by the chips of a MCM with high levels of mechanical stress from differential expansion and ultimate failure of the solder connections to the chip.

Claims 3 and 4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Turlik et al. (U.S. Patent # 5,325,265) in view of Hua (U.S. Patent Application Publication # 2004/0188503 A1).

Turlik et al. show for features of the claimed invention as detailed above, but fail to explicitly show the indium and the claimed alloys. However, Turlik et al. does discloses a solder joint **28** consisting essentially of indium **(see column 8, lines 50-63)** and optionally one or more alloying **(see column 8, lines 59-63)** constituents that increase the melting temperature of the solder joint above that of indium, the solder joint bonding the second surface of the device to the heat-conductive member. Specifically, Turlik et al. discloses the solder joint is pure indium is preferred because small additives of other materials (i.e. alloys of indium) can be used to decrease the creep rate for a given applied stress relative to pure (99.999 %) indium, thereby reducing compliance.

Hua is cited for showing solders with surfactant-refined grain sizes, solder bumps made thereof. Specifically, Hua (figures 1A to 7) specifically figure discloses solder composition of indium and silver, nickel in an amount of about 0.01 percent to about 3 percent **(see page 3, paragraph [0045] to [0050])** for the purpose of achieving some thermal expansion (CTE) matching.

3. The electronic assembly according to claim 1, the combination with Hua showing wherein the solder joint comprises indium and at least one of gold and **silver** in an amount of up to 0.5 weight percent **(see page 3, paragraph [0045] to [0047])**.
4. The electronic assembly according to claim 1, the combination with Hua showing wherein the solder joint comprising indium and at least one of **nickel**, nickel-gold alloy, tin, and tin alloy in an amount of up to 0.5 weight percent **(see page 4, paragraph [0048] to [0050])**.

Therefore, it would have been obvious to one of ordinary skill in the art to use Hua's solder composition to modify Turlik et al.'s solder joint for the purpose of achieving some thermal expansion (CTE) matching.

Claims 3 and 4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. (U.S. Patent # 6,423,570 B1) in view of Hua (U.S. Patent Application Publication # 2004/0188503 A1).

Ma et al. show for features of the claimed invention as detailed above, but fail to explicitly show the indium and the claimed alloys. However, Ma et al. does discloses a solder joint **115** consisting essentially of indium **(see column 4, lines 10-30)** and optionally one or more alloying **(see column 4, lines 15-21)** constituents that increase the melting temperature of the solder joint above that of indium, the solder joint bonding the second surface of the device to the heat-conductive member. Specifically, Ma et al. discloses the solder material, including, but not limited to, material such as a lead, **tin**, **indium**, gallium, bismuth, cadmium, zinc, copper, **gold, silver**, antimony, germanium, and **alloys thereof**.

Hua is cited for showing solders with surfactant-refined grain sizes, solder bumps made thereof. Specifically, Hua (figures 1A to 7) specifically figure discloses solder composition of indium and silver, nickel in an amount of about 0.01 percent to about 3 percent **(see page 3, paragraph [0045] to [0050])** for the purpose of achieving some thermal expansion (CTE) matching.

3. The electronic assembly according to claim 1, the combination with Hua showing wherein the solder joint comprises indium and at least one of gold and **silver** in an amount of up to 0.5 weight percent **(see page 3, paragraph [0045] to [0047])**.
4. The electronic assembly according to claim 1, the combination with Hua showing wherein the solder joint comprising indium and at least one of **nickel**, nickel-gold alloy, tin, and tin alloy in an amount of up to 0.5 weight percent **(see page 4, paragraph [0048] to [0050])**.

Therefore, it would have been obvious to one of ordinary skill in the art to use Ma et al.'s solder composition to modify Ma et al.'s solder joint for the purpose of achieving some thermal expansion (CTE) matching.

Claims 3 and 4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Koopman et al. (U.S. Patent # 4,081,825) in view of Hua (U.S. Patent Application Publication # 2004/0188503 A1).

Koopman et al. show for features of the claimed invention as detailed above, but fail to explicitly show the indium and the claimed alloys.

Hua is cited for showing solders with surfactant-refined grain sizes, solder bumps made thereof. Specifically, Hua (figures 1A to 7) specifically figure discloses solder composition of indium and silver, nickel in an amount of about 0.01 percent to about 3 percent **(see page 3, paragraph [0045] to [0050])** for the purpose of achieving some thermal expansion (CTE) matching.

3. The electronic assembly according to claim 1, the combination with Hua showing wherein the solder joint comprises indium and at least one of gold and **silver** in an amount of up to 0.5 weight percent **(see page 3, paragraph [0045] to [0047])**.
4. The electronic assembly according to claim 1, the combination with Hua showing wherein the solder joint comprising indium and at least one of **nickel**, nickel-gold alloy, tin, and tin alloy in an amount of up to 0.5 weight percent **(see page 4, paragraph [0048] to [0050])**.

Therefore, it would have been obvious to one of ordinary skill in the art to use Ma et al.'s solder composition to modify Kooperman et al.'s solder joint for the purpose of achieving some thermal expansion (CTE) matching.

Claims 3 and 4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Patel (U.S. Patent # 5,396,403) in view of Hua (U.S. Patent Application Publication # 2004/0188503 A1).

Patel et al. show for features of the claimed invention as detailed above, but fail to explicitly show the indium and the claimed alloys.

Hua is cited for showing solders with surfactant-refined grain sizes, solder bumps made thereof. Specifically, Hua (figures 1A to 7) specifically figure discloses solder composition of indium and silver, nickel in an amount of about 0.01 percent to about 3 percent **(see page 3, paragraph [0045] to [0050])** for the purpose of achieving some thermal expansion (CTE) matching.

3. The electronic assembly according to claim 1, the combination with Hua showing wherein the solder joint comprises indium and at least one of gold and **silver** in an amount of up to 0.5 weight percent **(see page 3, paragraph [0045] to [0047])**.

4. The electronic assembly according to claim 1, the combination with Hua showing wherein the solder joint comprising indium and at least one of **nickel**, nickel-gold alloy, tin, and tin alloy in an amount of up to 0.5 weight percent **(see page 4, paragraph [0048] to [0050])**.

Therefore, it would have been obvious to one of ordinary skill in the art to use Ma et al.'s solder composition to modify Patel's solder joint for the purpose of achieving some thermal expansion (CTE) matching.

Claims 3, 4, 14 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Koors et al. (U.S. Patent # 6,180,436 B1) in view of Patel (U.S. Patent # 5,396,403) and further in view of Hua (U.S. Patent Application Publication # 2004/0188503 A1).

The combination of Koors et al. and Patel et al. show for features of the claimed invention as detailed above, but fail to explicitly show the indium and the claimed alloys.

Hua is cited for showing solders with surfactant-refined grain sizes, solder bumps made thereof. Specifically, Hua (figures 1A to 7) specifically figure discloses solder composition of indium and silver, nickel in an amount of about 0.01 percent to about 3 percent **(see page 3, paragraph [0045] to [0050])** for the purpose of achieving some thermal expansion (CTE) matching.

3. The electronic assembly according to claim 1, the combination with Hua showing wherein the solder joint comprises indium and at least one of gold and **silver** in an amount of up to 0.5 weight percent **(see page 3, paragraph [0045] to [0047])**.
4. The electronic assembly according to claim 1, the combination with Hua showing wherein the solder joint comprising indium and at least one of **nickel**, nickel-gold alloy, tin, and tin alloy in an amount of up to 0.5 weight percent **(see page 4, paragraph [0048] to [0050])**.
14. The electronic assembly according to claim 13, the combination with Hua showing wherein the solder joint contains gold or silver in an amount of about 0.1 to about 0.5 weight percent **(see page 3, paragraph [0045] to [0047])**.

15. The electronic assembly according to claim 13, the combination with Hua showing wherein the solder joint contains one of nickel, nickel-gold alloy, tin, and tin alloy in an amount of about 0.1 to about 0.5 weight percent **(see page 4, paragraph [0048] to [0050])**.

Therefore, it would have been obvious to one of ordinary skill in the art to use Ma et al.'s solder composition to modify Ma et al.'s solder joint for the purpose of achieving some thermal expansion (CTE) matching.

Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Turlik et al. (U.S. Patent # 5,325,265) in view of Hua (U.S. Patent Application Publication # 2004/0188503 A1) and further in view of Deppisch et al. (U.S. Patent # 6,504,242 B1).

Turlik et al./Hua combination show for features of the claimed invention as detailed above, but fail to explicitly show the indium and the claimed alloys, wherein the solder joint consists essentially of indium, at least one of gold and silver in an amount of up to 0.5 weight percent, and at least one of nickel, nickel-gold alloy, tin and tin alloy in an amount of up to 0.5 weight percent. However, Turlik et al. does discloses a solder joint **28** consisting essentially of indium **(see column 8, lines 50-63)** and optionally one or more alloying **(see column 8, lines 59-63)** constituents that increase the melting temperature of the solder joint above that of indium, the solder joint bonding the second surface of the device to the heat-conductive member. Specifically, Turlik et al. discloses the solder joint is pure indium is preferred because small additives of other materials (i.e. alloys of indium) can be used to decrease the creep rate for a given applied stress relative to pure (99.999 %) indium, thereby reducing compliance.

Hua is cited for showing solders with surfactant-refined grain sizes, solder bumps made thereof. Specifically, Hua (figures 1A to 7) specifically figure discloses solder composition of indium and silver, nickel in an amount of about 0.01 percent to about 3 percent **(see page 3, paragraph [0045] to [0050])** for the purpose of achieving some thermal expansion (CTE) matching.

Deppisch et al. is cited for showing a electronic assembly having a wetting layer on a thermally conductive heat spreader. Specifically, Deppisch et al. (figures 1 to3)

specifically figure 3 discloses show the solder joint **22,24,52,46** consists essentially of **indium 14**, at least one of **gold 24** and silver, and at least one of **nickel 22**, **nickel-gold alloy 46**, tin and tin alloy for the purpose of providing a thermally conductive grease transfers minimal stresses from the heat spreader to the die.

Therefore, it would have been obvious to one of ordinary skill in the art to use Deppisch et al.'s thin amount of alloys, specifically nickel and Hua's solder composition of silver, nickel in an amount of about 0.01 percent to about 3 percent to modify Turlik et al.'s solder joint of pure (99.999 %) indium for the purpose of achieving some thermal expansion (CTE) matching and providing a thermally conductive grease transfers minimal stresses from the heat spreader to the die.

Claims 5 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Patel (U.S. Patent # 5,396,403) in view of Hua (U.S. Patent Application Publication # 2004/0188503 A1) and further in view of Deppisch et al. (U.S. Patent # 6,504,242 B1).

Patel et al./Hua show for features of the claimed invention as detailed above, but fail to explicitly show the indium and the claimed alloys, wherein the indium and the claimed alloys, wherein the solder joint consists essentially of indium, at least one of gold and silver in an amount of up to 0.5 weight percent, and at least one of nickel, nickel-gold alloy, tin and tin alloy in an amount of up to 0.5 weight percent.

Hua is cited for showing solders with surfactant-refined grain sizes, solder bumps made thereof. Specifically, Hua (figures 1A to 7) specifically figure discloses solder composition of indium and silver, nickel in an amount of about 0.01 percent to about 3 percent **(see page 3, paragraph [0045] to [0050])** for the purpose of achieving some thermal expansion (CTE) matching.

Deppisch et al. is cited for showing a electronic assembly having a wetting layer on a thermally conductive heat spreader. Specifically, Deppisch et al. (figures 1 to3) specifically figure 3 discloses show the solder joint **22,24,52,46** consists essentially of **indium 14**, at least one of **gold 24** and silver, and at least one of **nickel 22**, **nickel-gold alloy 46**, tin and tin alloy for the purpose of providing a thermally conductive grease transfers minimal stresses from the heat spreader to the die.

Therefore, it would have been obvious to one of ordinary skill in the art to use Deppisch et al.'s thin amount of alloys, specifically nickel and Hua's solder composition of silver, nickel in an amount of about 0.01 percent to about 3 percent to modify Patel's

solder joint of indium for the purpose of achieving some thermal expansion (CTE) matching and providing a thermally conductive grease transfers minimal stresses from the heat spreader to the die.

Claims 7 and 17, **insofar as claim 17 can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Patel (U.S. Patent # 5,396,403) in view of Smith (.S. Patent # 6,238,938 B1).

Patel show the features in the claimed invention as detailed above, but fail to explicitly show an overmold compound that encapsulates the substrate and the device on the housing member and underfills the flip-chip device.

Smith is cited for showing microelectronic connections with liquid conductive elements. Specifically, Smith (figures 1 to 23) specifically figure 20 discloses an overmold compound **1070** that encapsulates the substrate **1068** and the device **1022** on the housing member and underfills the flip-chip device for the purpose of providing protection and high reliability.

Therefore, it would have been obvious to one of ordinary skill in the art to use Smilth's encapsulation to modify Patel's assembly for the purpose of providing protection and high reliability.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/675,712,713,717,720,707,710,704,778,737,738,714	12/4/04
Other Documentation: foreign patents and literature in 257/675,712,713,717,720,707,710,704,778,737,738,714	12/4/04
Electronic data base(s): U.S. Patents EAST	12/4/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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